EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	430760	driv$3 near3 circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:14
L2	23	Plurality near3 (synchronous adj delay adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:05
L3	143	(synchronous adj delay adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:15
L4	3692	plurality near4 (delay adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:15
L5	10933	first near4 (delay adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:16
L6	1257	fourth near4 (delay adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:43
L7	72680	latch near3 circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:17

EAST Search History

L8	202	cascade near3 (IC or intergrat$3 adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:29
L9	446	cascade near3 (IC or integrat$3 adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:30
L10	1647223	(IC or integrat$3 adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:29
L11	8533	cascade near3 (circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:30
L12	6714	plurality near clock	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:30
L13	92	4 with 12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:30
L14	15	6 and 13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:33

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L15	11	10 and 14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:35
L16	987	5 and 6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:35
L17	223	7 and 16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:35
L18	2789	third near4 (delay adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:43
L19	11174	second near4 (delay adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:43
L20	2154	18 and 19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:43
L21	162	17 and 20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:43

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L22	19	12 and 21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:50
L23	114	1 and 17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:51
L24	78159	"345"/$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 15:52
L25	8	23 and 24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:02
L26	1	(phase adj adjustment adj circuit) and (synchronous adj delay) and (hold$3 adj circuit) and (clock)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:05
L27	1	(phase adj adjustment adj circuit) and (synchronous adj delay) and (clock)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:04
L28	1	(phase adj adjustment adj circuit) and (synchronous adj delay)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:04

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L29	82	(phase adj adjustment adj circuit) and (driv$3 adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:05
L30	143	(synchronous adj delay adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:06
L31	1	29 and 30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:06
L32	1	(synchronous adj delay) and 29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:06
L33	32	(delay adj circuit) and 29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:07
L34	18	10 and 33	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:16
L35	1	12 and 34	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:07

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L36	18	1 and 34	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:09
L37	27495	"713"/$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:17
L38	3	33 and 37	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:17

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L49	0	((drive adj circuit) with (phase adj adjustment adj circuit) with(driving adl display) with (inputting adj clock) and (phase adj adjustment adj circuit) with (first adj synchronous adj delay adj circuit) adj (input$4 adj clock) and (outputting adj first adj clock) with (second adj synchronous adj delay adj circuit) with (adjustting adj clock) with (outputting adj second adj clock) and (first adj holding adj circuit) and (first adj clock) and (second adj holding adj circuit) and (data adj output$4) with (first adj holding adj circuit) with (second adj clock) and (first adj phase adj adjustment adj circuit) with (first adj clock) and (first adj delay adj clock) and (latch adj circuit) with (output$4 adj data) with (first adj clock) and (third adj synchronous adj delay adj circuit) with (duty adj ratio) with (first adj clock) and (second adj clock) and (fourth adj synchronous adj delay adj circuit) with (second adj clock) and (output$4 adj second adj delay adj clock) and (second adj phase adj adjustment adj circuit) with (data input$3) with (second adj clock) and (second adj delay adj clock) with (output$4 adj data)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/17 16:52